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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/614,154	07/11/2000	Martin J. Edwards	PHB 34,365	1602

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EXAMINER	
SHAPIRO, LEONID	

ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 10/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/614,154	EDWARDS, MARTIN J.
	Examiner	Art Unit
	Leonid Shapiro	2673

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *1-8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9,10,12 and 13* is/are rejected.

7)☒ Claim(s) *11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. US Patent No. 6, 166, 715) in view of Enami et al. (US Patent no. 5,892,493).

As to claim 9, Chang et al. teaches an active matrix array device (See Col. 1, Lines 6-11) comprising:

a substrate (See Fig. 2, items 200-260, Col. 2, lines 20-29);

an array of individually addressable matrix elements carried on substrate (See Fig. 2, item 200);

a set of address conductors connected to array of matrix elements and carried on substrate (See Fig. 4, items PIX 1- PIX 40), set of address conductors being arranged in a series of groups with each group including successive address conductors (See Fig. 4, items PIX 1- PIX 640, Col. 5, Lines 18-49);

and an addressing circuit including

a multiplexing circuit (See Fig. 4, items EN1-EN16) integrated on substrate and connected to set of conductors, multiplexing circuit having a plurality of signal bus lines , multiplexing circuit being arrange to couple sequentially each group of set of address conductors to plurality of signal lines with each address conductor in a group being coupled to a respective one of signal bus lines (See Fig. 4, items PIX 1-PIX 640, Col. 5, Lines 18-49),

and a plurality of signal processing circuits (See Fig. 3, Items 245 (1)-245 (40)) integrated on substrate, each signal processing circuit connected to a respective bus line (See Fig. 3, items Y1-Y40, from Col. 3, Line 26 to col. 4, Line 3).

Matsueda et al. does not show a first signal processing circuit associated with a first address conductor of a first group of address conductor and a second signal processing circuit associated with a last address conductor of a second group of address conductors are adjacent on substrate.

Enami et al. teaches a first signal processing circuit (inside of multiplexer 38 and data line driver 40 in Fig. 1) associated with a first address conductor (d1B in Fig. 1) of a first group of address conductor (d1B-dnB in Fig. 1) and a second signal processing circuit (inside of multiplexer 38 and data line driver 40 in Fig. 1) associated with a last address conductor (dnA in Fig.1) of a second group of address conductors (d1A-dnA in Fig.1) are adjacent on substrate (See Col. 7, Lines 46-61).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching Enami et al. into the Chang et al. system in order to

selectively connect the driver to any one of sets data line groups (See Col. 2, Lines 8-15 in the Enami et al. reference).

As to claim 10, Chang et al. teaches signal processing circuits are arranged in series in a line parallel to multiplexing circuit (See Fig. 2-4, items 240, 260, Col. 3, Lines 26-47 and Col. 5, Lines 17-47).

2. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. and Enami et al. as applied to claim 9 above, and further in view of Matsueda et al. (US Patent 6, 384, 806).

Chang et al. and Enami et al. do not show an active matrix array device with order in which processing circuit blocks are arranged physically on the device substrate is different to the physical order of the signal bus lines to which they are respectively connected.

Matsueda et al. teaches an active matrix array device with order in which processing circuit blocks are arranged physically on the device substrate is different to the physical order of the signal bus lines to which they are respectively connected (See Fig. 17, items 200A, 200B, in description See Col.20, Lines 29-45). Notice that D/A converters on both sides of LCD panel.

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Matsueda et al. into Chang et al. and Enami et al. system in order to simplify circuit arrangement (See Col. 1, Lines 59-67).

3. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. in view of Matsueda et al.

Chang et al. teaches an active matrix array device (See Col. 1, Lines 6-11) comprising:

a substrate (See Fig. 2, items 200-260, Col. 2, lines 20-29);

an array of individually addressable matrix elements carried on substrate (See Fig. 2, item 200);

a set of address conductors connected to array of matrix elements and carried on substrate (See Fig. 4, items PIX 1- PIX 40), set of address conductors being arranged in a series of groups with each group including successive address conductors (See Fig. 4, items PIX 1- PIX 640, Col. 5, Lines 18-49);

and an addressing circuit including

a multiplexing circuit (See Fig. 4, items EN1-EN16) integrated on substrate and connected to set of conductors, multiplexing circuit having a plurality of signal bus lines , multiplexing circuit being arrange to couple sequentially each group of set of address conductors to plurality of signal lines with each address conductor in a group being coupled to a respective one of signal bus lines (See Fig. 4, items PIX 1-PIX 640, Col. 5, Lines 18-49),

and a plurality of signal processing circuits (See Fig. 3, Items 245 (1)-245 (40)) integrated on substrate, each signal processing circuit connected to a respective bus line (See Fig. 3, items Y1-Y40, from Col. 3, Line 26 to col. 4, Line 3).

Chang et al. do not show an order in which processing circuit blocks are arranged physically on the device substrate is different to the physical order of the signal bus lines to which they are respectively connected.

Matsueda et al. teaches an order in which processing circuit blocks are arranged physically on the device substrate is different to the physical order of the signal bus lines to which they are respectively connected (See Fig. 17, items 200A, 200B, Col.20, Lines 29-45). Notice that processing circuit blocks (D/A converters and other in the reference) are located on both sides of LCD panel.

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Matsueda et al. into Chang et al. system in order to simplify circuit arrangement (see Col. 1, Lines 59-67).

Allowable Subject Matter

4. Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is an examiner's statement of reasons for allowance:

Relative to claim 11, the major difference between the teaching of the prior art of record (Chang et al. and Enami et al.) and the instant invention is that the said prior art **does not teach** signal processing circuits are arranged in a first row and in a second row and offset from the first row in a brick-like fashion.

Response to Arguments

6. Applicant's arguments filed on 08-30-04 with respect to claim 9-10, 12-13 have been considered but are moot in view of the new ground(s) of rejection.

Telephone inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 703-305-5661. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-305-4938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ls 10-13-04

VIJAY SHANKAR
PRIMARY EXAMINER